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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/654,875	09/05/2000	Isao Nojiri	50006-073	7618

7590 09/25/2002

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EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	11

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.	Applicant(s)
09/654,875	Nojiri
Examiner	**Art Unit**
Nitin Parekh	2811

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Aug 19, 2002*.

2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *10-12* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) *10-12* is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *9 and 10*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 12 is rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 12, line 7 cites "...a wire connecting between the first pad and the second pad on the first semiconductor chip...".

However, the description in specification and Fig. 8 do not show a bonding wire connecting the pads.

Fig. 8 shows the trace/wire which is printed on the first semiconductor chip to provide an electrical connection between the first and second pad.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) in view of Fukui et al (US Pat. 6100594) and Williams et al (US Pat. 5665996).

Regarding claim 10, the APA discloses a semiconductor device mounted on a mother board comprising:

- a circuit board (102 in Fig. 11/12) to be positioned on the mother board

- semiconductor chips (110, 112, etc. in Fig. 11/12) positioned on the circuit board, wherein

a) the circuit board has a second pad/connection pads (104-1, 104-2, etc. in Fig. 11/12) spaced away from each other

b) the semiconductor chip (112 in Fig. 11/12) has connection pads/a third pad positioned adjacent/corresponding to the second pad/connection pads formed on the surface of the circuit board, and

c) the second pad on the circuit board and the third pad on the chip are electrically connected through a bonding wire (116 in Fig. 11/12)

(Specification pp. 1-4; Fig. 11 and 12).

The APA fails to specify using the circuit board having a first and second pads such that the second pad is spaced away from the first pad in a direction along outer peripheral edge of the chip and a wire being printed on the board, the wire connecting the first and second pad.

Fukui et al teach using pads on the circuit board comprising an elongated pad (13 showing two bonding wires in Fig. 7a) which has an inner/first pad and an outer/second pad (not numerically referenced in Fig. 7a) and they are connected with a wire portion/printed wiring trace (Col. 10, line 30-42). Fukui et al further teach forming the first/second pads being spaced away from each other in any direction along/perpendicular (X/Y) with respect to the outer peripheral edges of the chip (pad 13/17a in Fig. 7a/9a respectively; Col. 10).

Furthermore, Fukui et al teach forming the wiring portion/trace pattern using conventional deposition and photolithography/printing processes (Col. 7, line 30-60).

Williams et al teach using a conventional bonding wire (Fig. 6A/B) to connect the desired wiring portions (Col. 2, line 58).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a circuit board having a first and second pads such that the second pad is spaced away from the first pad in a direction along outer peripheral edge of the chip and a wire being printed on the board connecting the first and second pad so that wire bonding defects, bonding wire length wire-shorting problems can be reduced using Fukui et al and Williams et al's wiring design in the APA.

5. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukui et al (US Pat. 6100594) in view of Williams et al (US Pat. 5665996) and Bertin et al (US Pat. 6294406).

Regarding claim 11, Fukui et al disclose a semiconductor device comprising:

a) a first semiconductor chip (1 in Fig. 7b) having connection pads/second pad (17a in Fig. 7b)

b) a second semiconductor chip positioned on the first chip and having connection pads/third pad (17b in Fig. 7b) positioned adjacent to the second pad, and

c) the second pad on the first chip being electrically connected with the third pad on the second chip through a bonding wire (7 in Fig. 7b)

(Fig. 7b; Fig. 6a-9b; Col. 10, line 12-66).

Fukui et al fail to specify using the first chip having a first and second pads such that the second pad is spaced away from the first pad in a direction along outer peripheral edge of the chip and a wire being printed on the board so that the third pad is electrically connected to the first and second pad through the bonding wire and printed wire.

However, Fukui et al further teach using pads on the first chip comprising an elongated pad (17a in Fig. 9a) which has an inner/first pad and an outer/second pad (not numerically referenced in Fig. 9a) and they are connected with a wire portion/printed wiring trace (Col. 10, line 30-42). Furthermore, the first/second pads are spaced away from each other in any direction along/perpendicular (X/Y) with respect to the outer peripheral edges of the chip (pad 17a/13 in Fig. 9a/7a respectively; Col. 10).

Fukui et al further teach forming the wiring portion/trace pattern using conventional deposition and photolithography/printing processes (Col. 7, line 30-60).

Williams et al teach using a conventional bonding wire (Fig. 6A/B) to connect the desired wiring portions (Col. 2, line 58).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a first chip having a first and second pads such that the second pad is spaced away from the first pad in a direction along outer peripheral edge of the chip and a wire being printed on the board so that the third pad is electrically connected to the first and second pad through the bonding wire and printed wire resulting in reduced wire bonding defects and bonding wire length/shorting problems using and Williams et al's wiring design in Fukui et al's device.

Regarding claim 12, as explained above for claim 11, Fukui et al fail to specify using the second chip having the third pad in the region such that the third pad faces the first pad of the first chip and is being electrically connected using a conductive member positioned between the first pad and third pad.

Bertin et al teach connecting the second chip positioned on the first chip using conventional flip chip bonding (40/30 in Fig. 5) such that a conductive member/metal/solder pads of the first and second chips are in a region facing each other and are electrically connected through conventional interconnections including wiring/traces, conductive member/solder ball (50 in Fig. 5) positioned in the active region of the chip (Col. 3, line 1-66).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate a second chip having the third pad in the region such that the third pad faces the first pad of the first chip and is being electrically connected using a conductive member positioned between the first pad and third pad so that interconnection density can be improved and the package dimensions can be reduced using Bertin et al and Williams et al's wiring design in Fukui et al's device.

Response to Arguments

6. Applicant's arguments filed on 08-19-02 have been fully considered but they are not persuasive.

A. Applicant contends that Bertin et al do not cure the deficiencies of the APA and Fukui et al.

As explained above, Fukui et al fail to specify using a flip chip/face down bonding for the second chip. However, Bertin et al teach using a conventional flip chip bonding (Fig. 5; Col. 3) where the second chip is positioned on the first chip and is being electrically connected through conventional conductive elements such as wiring/circuit traces, solder balls, bumps, etc. Therefore, Bertin et al's bonding structure is applied to Fukui et al's device.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted directly to Art Unit 2811 by facsimile transmission. Papers should be faxed to Art Unit via Technology Center 2800 fax center located in Crystal Plaza 4, room 4C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (15 November 1989).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number in (703) 305-3410. The examiner can be normally reached on Monday-Friday from 08:30 am-5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached on (703) 308-2772. The fax number for the organization where this application or proceeding is assigned is (703) 308-7722 or 7724.

Nitin Parekh

09-17-02

Steven Loke

Steven Loke